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APPLICATION NO.	FILING DATE	FIRST NAMED INVENTOR	ATTORNEY DOCKET NO.	CONFIRMATION NO.
09/489,652	01/24/2000	William G. Burroughs	KUC-718US	6089
46900 7590 01/10/2008 MENDELSON & ASSOCIATES, P.C. 1500 JOHN F. KENNEDY BLVD., SUITE 405 PHILADELPHIA, PA 19102			EXAMINER TANG, KENNETH	
			ART UNIT 2195	PAPER NUMBER
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Please find below and/or attached an Office communication concerning this application or proceeding.

The time period for reply, if any, is set in the attached communication.

Office Action Summary

Application No.

09/489,652

Applicant(s)

BURROUGHS ET AL.

Examiner

Kenneth Tang

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-- The MAILING DATE of this communication appears on the cover sheet with the correspondence address --

Period for Reply

A SHORTENED STATUTORY PERIOD FOR REPLY IS SET TO EXPIRE 3 MONTH(S) OR THIRTY (30) DAYS, WHICHEVER IS LONGER, FROM THE MAILING DATE OF THIS COMMUNICATION.

- Extensions of time may be available under the provisions of 37 CFR 1.136(a). In no event, however, may a reply be timely filed after SIX (6) MONTHS from the mailing date of this communication.
- If NO period for reply is specified above, the maximum statutory period will apply and will expire SIX (6) MONTHS from the mailing date of this communication.
- Failure to reply within the set or extended period for reply will, by statute, cause the application to become ABANDONED (35 U.S.C. § 133). Any reply received by the Office later than three months after the mailing date of this communication, even if timely filed, may reduce any earned patent term adjustment. See 37 CFR 1.704(b).

Status

- 1) ☒ Responsive to communication(s) filed on 16 July 2007.
- 2a) ☒ This action is **FINAL**. 2b) ☐ This action is non-final.
- 3) ☐ Since this application is in condition for allowance except for formal matters, prosecution as to the merits is closed in accordance with the practice under *Ex parte Quayle*, 1935 C.D. 11, 453 O.G. 213.

Disposition of Claims

- 4) ☒ Claim(s) 27,29-38 and 40-58 is/are pending in the application.
- 4a) Of the above claim(s) _____ is/are withdrawn from consideration.
- 5) ☒ Claim(s) 53-58 is/are allowed.
- 6) ☒ Claim(s) 27,30,34-38,41,45,46 and 49-51 is/are rejected.
- 7) ☒ Claim(s) 29, 31-33, 40, 42-44, 47-48, and 52 is/are objected to.
- 8) ☐ Claim(s) _____ are subject to restriction and/or election requirement.

Application Papers

- 9) ☐ The specification is objected to by the Examiner.
- 10) ☐ The drawing(s) filed on _____ is/are: a) ☐ accepted or b) ☐ objected to by the Examiner.
- Applicant may not request that any objection to the drawing(s) be held in abeyance. See 37 CFR 1.85(a).
- Replacement drawing sheet(s) including the correction is required if the drawing(s) is objected to. See 37 CFR 1.121(d).
- 11) ☐ The oath or declaration is objected to by the Examiner. Note the attached Office Action or form PTO-152.

Priority under 35 U.S.C. § 119

- 12) ☐ Acknowledgment is made of a claim for foreign priority under 35 U.S.C. § 119(a)-(d) or (f).
- a) ☐ All b) ☐ Some * c) ☐ None of:
1. ☐ Certified copies of the priority documents have been received.
2. ☐ Certified copies of the priority documents have been received in Application No. _____.
3. ☐ Copies of the certified copies of the priority documents have been received in this National Stage application from the International Bureau (PCT Rule 17.2(a)).

* See the attached detailed Office action for a list of the certified copies not received.

Attachment(s)

- 1) ☒ Notice of References Cited (PTO-892)
- 2) ☐ Notice of Draftsperson's Patent Drawing Review (PTO-948)
- 3) ☐ Information Disclosure Statement(s) (PTO/SB/08)
Paper No(s)/Mail Date _____
- 4) ☐ Interview Summary (PTO-413)
Paper No(s)/Mail Date. _____
- 5) ☐ Notice of Informal Patent Application
- 6) ☐ Other: _____

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DETAILED ACTION

1. The finality of the Office actions mailed 7/31/07 and 5/22/07 are hereby withdrawn in view of the new ground of rejection set forth below. Applicant's amendment on 2/22/07 necessitated the new ground(s) of rejection presented in this Office action.
2. Claims 27, 29-38, and 40-58 are presented for Examination.

Allowable Subject Matter

3. Claims 29, 31-33, 40, 42-44, 47-48, and 52 are objected to as being dependent upon a rejected base claim, but would be allowable if rewritten in independent form including all of the limitations of the base claim and any intervening claims.
4. Claims 53-58 are allowed.

Claim Rejections - 35 USC § 102

The following is a quotation of the appropriate paragraphs of 35 U.S.C. 102 that form the basis for the rejections under this section made in this Office action:

A person shall be entitled to a patent unless –

(e) the invention was described in (1) an application for patent, published under section 122(b), by another filed in the United States before the invention by the applicant for patent or (2) a patent granted on an application for patent by another filed in the United States before the invention by the applicant for patent, except that an international application filed under the treaty defined in section 351(a) shall have the effects for purposes of this subsection of an application filed in the United States only if the international application designated the United States and was published under Article 21(2) of such treaty in the English language.

5. **Claims 27, 30, 36-38, 41, 49-51 are rejected under 35 U.S.C. 102(e) as being anticipated by Falik et al (US 6,065,078).**

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6. As per claim 27, Falik et al teach a system comprising a first processor (1840a, fig. 21) and one or more other processors (1840b, 1840c), a method for applying one or more interrupt signals (1848a, 1848b, 1848c) to the one or more other processors, the method comprising:

(a) generating, in the first processor, a data word having two or more data bits¹ (col. 16, lines 40 – 42), wherein each data bit has either a first bit value (1) or a second bit value (0);

(b) transmitting the data word from a data port of the first processor to a signal unit (1841) external to the first processor and the one or more other processors;

(c) converting, in the signal unit, the data word into one two or more interrupt signals by analyzing the bit value of each of two or more data bits in the data word, wherein each analyzed data bit in the data word having a specified bit value corresponds to a different interrupt signal (col. 16, lines 1 – 7, fig.14); and

(d) transmitting each interrupt signal from the signal unit to an interrupt port of an other processor (col. 16, lines 43 – 45).

“The debugger interface module 1841 has an interrupt connection (1848a through 1848c) to each of the processor cores (1840a to 1840c)”, col.2, lines 55 - 57.

“The debugger interface module 1841 supports four operations: RX session, TX session, chip RESET, and ABORT. Some of these operations can be simultaneously active for the same, or different, processors 1840a to 1840c.”, col. 4, lines 25 – 29.

¹ A detail discussion is set forth hereinbelow.

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“Now, the registers of the debugger interface module 1841, as they appear to the processor cores 1840a to 1840c, are discussed. The processor cores can perform read and/or write operations to the debuggers 1830a to 1830c using these registers. The registers should be accessible using memory and I/O operations.”, col. 14, lines 60 – 65.

“DBGABORT is the debug abort generate register, a word-wide, write-only register, used to generate an ABORT. A processor 1840a to 1840c may generate an ABORT to a processor with a PID index of i, by modifying its P.sub.-- i bit to 1. Writing 0 to P.sub.-- i does not result in ISE interrupt assertion to that processor 1840a to 1840c. The DBGABORT register format is shown in FIG. 14.”, col. 16, lines 1 – 7.

“When one core 1840a to 1840c reaches a breakpoint, it can break all the other cores or a subset of them. The JTAG controlled ABORT mask register defines which of the processors 1840a to 1840c will be stopped at a general abort. When the core reaches the breakpoint it will write to the DBGABORT register a “1” to the position of all processors 1840a to 1840c it needs to stop (usually all except itself). As a result, an ISE interrupt will be sent to all the processors whose respective bit in the ABORT register is set 1840a to 1840c and their program flow will be interrupted. Note that if the processor is already executing within monitor code, there will be no ISE interrupt and only the ABORT bit will be set. The monitor of each stopped processor will need to respond to the ISE interrupt the next time it polls on DBGISESRCA register. (Note that even though there is a delay in the response here, the application is not running and only monitor code is executed during this window). The purpose of this mechanism is to prevent nested calls to the monitor.”, (emphasis added by the examiner), col. 16, lines 36 – 54.

Falik et al do not explicit teach the generating a data word having two or more data bits. However, the examiner submits that, inherently, Falik et al generate a data word having two or more data bits for the reasons set forth hereinbelow.

To support this, either a TAP 102 instruction issued by the host or a bitset operation in the DBGABORT register issued by one or the other processors need to be executed. In response, processor 1840a to 1840c receive an unmaskable interrupt from ISE interrupt control 104 to stop its execution. Either of these causes the processor to assert a non-zero. BGISESRC.ABORT.sub.-- I bit to indicate that an ABORT event occurred, which causes the ABORT. (emphasis added by the examiner) (col. 5, lines 9 – 16.)

DBGABORT is the debug abort generate register, a word-wide, write-only register, used to generate an ABORT. A processor 1840a to 1840c may generate an ABORT to a processor with a PID index of i, by modifying its P.sub.-- i bit to 1. Writing 0 to P.sub.-- i does not result in ISE interrupt assertion to that processor 1840a to 1840c. The DBGABORT register format is shown in FIG. 14. (emphasis added by the examiner)

P.sub.-- i of DBGABORT indicates the ABORT source activation.

0: Processor ID i does not get an ABORT.

1: Processor ID i gets an ABORT. (col. 16, lines 1 – 11)

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An ABORT event occurs when SCAN.sub.-- RX is executed with a PID of all 1's (ISE and DBGISESRC.ABORT.sub.-- bits are asserted), or when a processor's bits P.sub.-- i are set in the DBGABORT register by one of the processors (i.e., ISE and DBGISESRC bits are asserted with the write operation itself). If DBGABORT is written with some zero bits, the PIDs that correspond to these zero bits do not get the ISE interrupt). In an ABORT event, the assertion of each ISE interrupt and DBGISESRC bit depends on the masking bit, corresponding to that ISE interrupt, at the DBGMASKS shift register. (emphasis added by the examiner) (col. 7, lines 38 – 48)

A bitset operation is used by any processor to set the bits in the DBGABORT register. The reference does not explicitly provide the details of the bitset operation. The examiner submits that, inherently, all the bits are set in the same bitset operation². In other words, each of the processors can directly write a 0 to any bit in the DBGABORT register. Each of the processors writes all the bits in the same bitset operation.

Specifically, if the DBGABORT register has 4 bits, there are two methods to write to the register:

1. Write to each bit individually.

for example : write reg1 (bit 1) = 0/1
 write reg1 (bit 2) = 0/1
 write reg1 (bit 3) = 0/1
 write reg1 (bit 4) = 0/1

It takes n cycles to write n bits into the register.

2. Write a word to address each of the bits concurrently

write reg1 = 1100 or 0110... etc.

It takes ONE (1) cycle to write 4 bits into the register.

In the default condition, the DBGABORT register has information 0000 (nothing is to be stopped by default). If a processor wants to change first and last bits to 1 to stop the first and fourth processors, the following operations will be performed based upon the first method:

write reg1 (bit 1) = 1
 write reg1 (bit 4) = 1

The processor will never write a 0 to the bit because the default bit value is 0 (no interrupt). At most, the processor resets the register to get all the bits to 0. In the running state, a

² According to the claimed limitation, it is generating a data word having two or more data bits.

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processor only writes a 1 to a register bit. If the processor writes a 0 to a register bit already has a value 0, it is because the processor using the second method, i.e. write to all the register bits as a word in a single cycle.

As a word, the processor has to set each of bits in the DBGABORT register without ignoring some of the bits. If the processor's respective bit is originally 0 and no interrupt is intended for the same processor, a processor having control of the DBGABORT register still need to write a 0 in the same bit position of the word. The processor performs the following write operation based upon the second method:

write reg1= 1001

After serving the interrupts to the appropriate processors, the DBGABORT register has to be reset to all 0 (the default value). If the current value (for example 1001) is stayed in the register after the interrupt, a next processor, any processor n, comes along and set bits 2 and 3 to 1. The resultant value of the DBGABORT register is 1111. Processor n can't set the first and fourth bits to 0 because it doesn't care about the bit values of the DBGABORT register prior to its own bitset operation. As such, the DBGABORT register has to be reset after each interrupt operation.

In summary, in order to allow the writing of 0 to a register bit which is 0 by default, it is the examiner's position that the bitset operation (col. 5, line 10), inherently, has to write a plurality of bits concurrently as a word - generating a data word having two or more data bits

7. As to claim 30, Falik et al. teaches wherein at least two interrupt signals are transmitted to interrupt ports of at least two different other processors (Fig. 21, 1841, 1840a, 1840b, 1840c, etc.).

8. As to claim 36, it is rejected for the same reason as stated in the rejection of claim 27.

Falik et al. teaches two-way communication between the processors (see Fig. 21, 1840a, 1840b, 1840c, etc.).

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9. As to claim 37, Falik et al. teaches wherein at least one other interrupt signal is transmitted from the other signal unit to an interrupt port of at least one other processor (Fig. 21, 1841, 1840a, 1840b, 1840c, etc.) because Falik et al. teaches two-way communication between the processors.

10. As to claims 38, it is rejected for the same reasons as stated in the rejection of claims 27.

11. As to claims 41, it is rejected for the same reasons as stated in the rejection of claim 30.

12. As to claims 49-50, they are rejected for the same reasons as stated in the rejections of claims 1 and 35.

13. As to claim 51, it is rejected for the same reasons as stated in the rejection of claim 27.

Claim Rejections - 35 USC § 103

The following is a quotation of 35 U.S.C. 103(a) which forms the basis for all obviousness rejections set forth in this Office action:

(a) A patent may not be obtained though the invention is not identically disclosed or described as set forth in section 102 of this title, if the differences between the subject matter sought to be patented and the prior art are such that the subject matter as a whole would have been obvious at the time the invention was made to a person having ordinary skill in the art to which said subject matter pertains. Patentability shall not be negated by the manner in which the invention was made.

14. **Claims 34-35 and 45-46 are rejected under 35 U.S.C. 103(a) as being unpatentable over Falik et al (US 6,065,078) in view of Arimilli (US 6,275,502 B1).**

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15. As to claim 34, Falik et al. teaches wherein each interrupt signal is transmitted from the signal unit to a corresponding interrupt port of a corresponding other processor (see rejection of claim 27). Falik et al. is silent in teaching that a dedicated line is used for this communication. However, Arimilli teaches that connections made from one site to another site over a composite link using a dedicated line is an efficient use of the line resources (col. 2, lines 34-36). Therefore, it would have been obvious to one of ordinary skill in the art at the time the invention was made to include the feature of a dedicated line to the existing system of Falik because it would provide the predicted result of an efficient communication line for communication between the processors (col. 2, lines 34-36).

16. As to claim 35, Falik et al. teaches wherein the data word is transmitted from the first processor to the signal unit via a shared data bus (Fig. 21, 1846, Fig. 16, 116).

17. As to claims 45-46, they are rejected for the same reasons as stated in the rejections of claims 34-35.

Response to Arguments

18. *Applicant argues the finality of the rejection.*

19. In response, the final rejection of 5/22/07 was replaced with a new final rejection on 7/31/07. Furthermore, the previous final rejection is being replaced with this current final office

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action. Applicant's amendment on 2/22/07 necessitated the new ground(s) of rejection presented in this Office action. Therefore, a third final office action is replacing the prior office actions.

20. Applicant's arguments have been fully considered but are moot in view of the new grounds of rejections.

Conclusion

21. Applicant's amendment on 2/22/07 necessitated the new ground(s) of rejection presented in this Office action. Accordingly, **THIS ACTION IS MADE FINAL**. See MPEP § 706.07(a). Applicant is reminded of the extension of time policy as set forth in 37 CFR 1.136(a).

A shortened statutory period for reply to this final action is set to expire THREE MONTHS from the mailing date of this action. In the event a first reply is filed within TWO MONTHS of the mailing date of this final action and the advisory action is not mailed until after the end of the THREE-MONTH shortened statutory period, then the shortened statutory period will expire on the date the advisory action is mailed, and any extension fee pursuant to 37 CFR 1.136(a) will be calculated from the mailing date of the advisory action. In no event, however, will the statutory period for reply expire later than SIX MONTHS from the date of this final action.

Any inquiry concerning this communication or earlier communications from the examiner should be directed to Kenneth Tang whose telephone number is (571) 272-3772. The examiner can normally be reached on 8:30AM - 6:00PM, Every other Friday off.

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If attempts to reach the examiner by telephone are unsuccessful, the examiner's supervisor, Meng-Ai An can be reached on (571) 272-3756. The fax phone number for the organization where this application or proceeding is assigned is 571-273-8300.

Information regarding the status of an application may be obtained from the Patent Application Information Retrieval (PAIR) system. Status information for published applications may be obtained from either Private PAIR or Public PAIR. Status information for unpublished applications is available through Private PAIR only. For more information about the PAIR system, see <http://pair-direct.uspto.gov>. Should you have questions on access to the Private PAIR system, contact the Electronic Business Center (EBC) at 866-217-9197 (toll-free). If you would like assistance from a USPTO Customer Service Representative or access to the automated information system, call 800-786-9199 (IN USA OR CANADA) or 571-272-1000.

Kt

11/20/07

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